Electronic Version
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Claims

[c1] What is claimed is:

1. A bipolar junction transistor, comprising:

a substrate;

a dielectric layer formed on the substrate;

an opening formed in the dielectric layer to expose a portion of the substrate;

a semiconductor layer formed on a sidewall and a bottom of the opening, the semiconductor layer extending outside the opening and above the dielectric layer;

a spacer formed on the semiconductor layer to define a self-aligned emitter region in the opening;

an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the semiconductor layer; and

a salicide layer formed on the emitter conductivity layer and on the portion of the semiconductor layer extending outside the opening and above the dielectric layer.

[c2] 2. The bipolar junction transistor of claim 1, wherein the semiconductor layer comprises at least one material selected from a material group consisting of silicon epi-

taxy, GaAs, InP and AlGaAs.

[c3] 3. The bipolar junction transistor of claim 1, further comprising a selective implant collector region formed in the substrate beneath the semiconductor layer.

[c4] 4. The bipolar junction transistor of claim 1, further comprising an extended conductivity layer formed on the dielectric layer to connect to the semiconductor layer.

[c5] 5. The bipolar junction transistor of claim 4, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

[c6] 6. The bipolar junction transistor of claim 4, wherein the extended conductivity layer is composed of polysilicon.

[c7] 7. A hetero-junction bipolar junction transistor, comprising:
a substrate;
a dielectric layer formed on the substrate;
an opening formed in the dielectric layer to expose a portion of the substrate;
a GaAs layer formed on a sidewall and a bottom of the opening;
a spacer formed on the GaAs layer to define a self-aligned emitter region in the opening; and

an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the GaAs layer.

[c8] 8. The hetero-junction bipolar junction transistor of claim 7, further comprising a selective implant collector region formed in the substrate beneath the GaAs layer.

[c9] 9.The hetero-junction bipolar junction transistor of claim 7, wherein the GaAs layer extends outside the opening and above the dielectric layer.

[c10] 10. The hetero-junction bipolar junction transistor of claim 9, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the GaAs layer extending outside the opening and above the dielectric layer.

[c11] 11. The hetero-junction bipolar junction transistor of claim 7, further comprising an extended conductivity layer formed on the dielectric layer to connect to the GaAs layer.

[c12] 12. The hetero-junction bipolar junction transistor of claim 11, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

[c13] 13. The hetero-junction bipolar junction transistor of claim 11, wherein the extended conductivity layer is composed of polysilicon.

[c14] 14. A hetero-junction bipolar junction transistor, comprising:
a substrate;
a dielectric layer formed on the substrate;
an opening formed in the dielectric layer to expose a portion of the substrate;
a InP layer formed on a sidewall and a bottom of the opening;
a spacer formed on the InP layer to define a self-aligned emitter region in the opening; and
an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the InP layer.

[c15] 15. The hetero-junction bipolar junction transistor of claim 14, further comprising a selective implant collector region formed in the substrate beneath the InP layer.

[c16] 16. The hetero-junction bipolar junction transistor of claim 14, wherein the InP layer extends outside the opening and above the dielectric layer.

[c17] 17. The hetero-junction bipolar junction transistor of

claim 16, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the InP layer extending outside the opening and above the dielectric layer.

[c18] 18. The hetero-junction bipolar junction transistor of claim 14, further comprising an extended conductivity layer formed on the dielectric layer to connect to the InP layer.

[c19] 19. The hetero-junction bipolar junction transistor of claim 18, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

[c20] 20. The hetero-junction bipolar junction transistor of claim 18, wherein the extended conductivity layer is composed of polysilicon.

[c21] 21. A hetero-junction bipolar junction transistor, comprising:
a substrate;
a dielectric layer formed on the substrate;
an opening formed in the dielectric layer to expose a portion of the substrate;
an AlGaAs layer formed on a sidewall and a bottom of the opening;

a spacer formed on the AlGaAs layer to define a self-aligned emitter region in the opening; and
an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the AlGaAs layer.

[c22] 22. The hetero-junction bipolar junction transistor of claim 21, further comprising a selective implant collector region formed in the substrate beneath the AlGaAs layer.

[c23] 23. The hetero-junction bipolar junction transistor of claim 21, wherein the AlGaAs layer extends outside the opening and above the dielectric layer.

[c24] 24. The hetero-junction bipolar junction transistor of claim 23, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the AlGaAs layer extending outside the opening and above the dielectric layer.

[c25] 25. The hetero-junction bipolar junction transistor of claim 21, further comprising an extended conductivity layer formed on the dielectric layer to connect to the Al-GaAs layer.

[c26] 26. The hetero-junction bipolar junction transistor of claim 25, further comprising an oxide layer and a silicon

nitride layer formed between the extended conductivity layer and the dielectric layer.

[c27] 27. The hetero-junction bipolar junction transistor of claim 25, wherein the extended conductivity layer is composed of polysilicon.